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10/766,768	01/27/2004	Ronald Duane McCallister	2298-010	3629

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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,768	MCCALLISTER, RONALD DUANE	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed on 1/27/04 and 5/10/04 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the references under the "Non patent Literature Documents " do not show the appropriate filing or publication date. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 11-16, 18, 20, 22, 24 29-30, 32-34, 36-37, 45-46, 50, 54, 57-58, 61-63 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Rahman et al U.S. Pub No 2003/0174783 A1.

As per claims 1, 30, and 45 Rahman et al teaches a predistortion circuit for compensating linear distortion introduced by analog-transmitter components of a digital communications transmitter, said predistortion circuit comprising: a source of a complex-forward-data stream configured to digitally convey information (see fig.2 element 86 and page 2 [0020]; a digital equalizer section coupled to said complex-forward-data-stream source and configured to generate an equalized-complex-forward-data stream and to pass said equalized-complex-forward-data stream to said analog-transmitter components (see fig.2 elements 90, 88 and page 2 [0020] and page [0024]); a feedback section adapted to receive a feedback signal from said analog-transmitter components and configured to provide a complex-return-data stream (see abstract and fig.2 elements 38, 82, 84 and page 2 [0018], [0023]) ; and a controller (see fig.2 element 76 and page 2 [0023] and page 3 [0029] and page 4 [0036]) coupled to said feedback section and to said equalizer section and configured so that said equalizer section (fig.2 elements 38, 82, 84) compensates for frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components (see page 2 [0018] and page 3 [0027] and page 4 [0034]).

As per claims 2, Rahman et al inherently teaches a predistortion circuit as claimed in claim 1 wherein said analog-transmitter components include a power amplifier having an input and an output (see page 1 [0005-0006]), and said feedback

section comprises: a first analog input (see fig.2 element 52) adapted to receive a first RF-analog signal from said power amplifier input; and a second analog input (see fig.2 element 44) adapted to receive a second RF- analog signal from said power amplifier output.

As per claims 11, Rahman et al teaches predistortion circuit as claimed in claim 1 wherein said equalizer section implements a complex equalizer (see fig.1 element 90 or 88).

As per claims 12, 32, 39 Rahman et al inherently teaches predistortion circuit as claimed in claim 1 wherein: said complex-forward-data stream exhibits a forward resolution (see fig.2 element 36); and said complex-return-data stream exhibits a return resolution less than said forward resolution (see fig.2 element 38).

As per claims 13, 33, 40 Rahman et al inherently teaches predistortion circuit as claimed in claim 12 wherein said feedback section generates said complex-return- data stream so that said return resolution is at most four bits less than said forward resolution.

As per claims 14, Rahman et al inherently teaches predistortion circuit as claimed in claim 1 wherein said feedback section comprises a complex-digital-subharmonic- sampling downconverter adapted to receive said feedback signal from said analog-transmitter components and configured to provide said complex-return-data stream.

As per claims 15, 34, 36, 42, 57 Rahman et al inherently teaches, predistortion circuit as claimed in claim 1 additionally comprising a programmable register is the

same as the claimed (programmable delay element) coupled between said complex-forward-data-stream source and said feedback section, said programmable delay element being configured to produce a delayed-complex-forward-data stream temporally aligned with said complex-return-data stream (see page 3 [0027] and page 4 [00036] and page 5 [0047]).

As per claims 16, 37 Rahman et al inherently teaches, a predistortion circuit as claimed in claim 15 wherein: said complex-forward-data stream propagates through said predistortion circuit in response to a clock signal (see fig.2 element 76); and said a programmable register is the same as the claimed (programmable delay element) includes an integral section that delays at least a portion of said complex-forward- data stream by an integral number of cycles of said clock signal and includes a fractional section that delays said portion of said complex-forward-data stream by a fraction of a cycle of said clock signal(see page 3 [0027] and page 4 [00036]).

As per claims 18, 58 Rahman et al inherently teaches a predistortion circuit as claimed in claim 15 wherein said controller is configured to cause said a programmable register is the same as the claimed (programmable delay element) to temporally align said delayed- complex-forward-data stream with said complex-return-data stream prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components (see page 3 [0027] and page 4 [00036] and page 5 [0047]).

As per claims 20, 61 Rahman et al inherently teaches predistortion circuit as claimed in claim 1 wherein: said analog-transmitter components include a band-pass

filter (see fig.2 element 98 or 1000 or 46 or 54) which inserts a band-pass-filter delay; and said predistortion circuit additionally comprises a phase rotator (see page 5 [0042]) configured to rotate one of said complex-forward-data and complex-return-data streams relative to the other to compensate for said band-pass-filter delay.

As per claims 22, 62Rahman et al inherently teaches predistortion circuit as claimed in claim 20 wherein said controller is configured to cause said phase rotator(see page 5 [0042]) to compensate for said band-pass-filter delay prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

As per claims 24, 65 Rahman et al inherently teaches A predistortion circuit as claimed in claim 1 wherein said equalizer section includes a first equalizer (see fig.2 element 90) configured to filter said complex-forward-data stream and a second equalizer (see fig.2 element 88) configured to filter said complex-return-data stream.

As per claims 29, Rahman et al inherently teaches A predistortion circuit as claimed in claim 24 wherein: said analog section includes a power amplifier(see page 1 [0005-0006]), which exhibits a gain; and said predistortion circuit additionally comprises an adjustable attenuation circuit configured to compensate for said gain of said power amplifier and positioned to process said complex-return-data stream before filtering in said second equalizer (see page 1 [0006-0007] and page 2 [0021] and page 3 [0031]).

As per claims 46, Rahman et al inherently teaches: said quadrature-balancing activity is performed by an equalizer section (see fig.2 element 90 or 88); and said

processing activity compensates for frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components (see abstract).

As per claims 50, Rahman et al inherently teaches wherein said equalizer section includes a first equalizer (see fig.2 element 90) configured to filter said complex-forward-data stream and produce said balanced-complex-forward-data stream and includes a second equalizer (see fig.2 element 88) configured to filter said complex-return-data stream.

As per claim 54, Rahman et al inherently teaches wherein said down- converting activity is performed by a digital-sub-harmonic- sampling down-converter.

As per claim 63, Rahman et al inherently teaches method as claimed in claim 45 wherein: said analog-transmitter components include a power amplifier which is driven by a power-amplifier-input signal and which produces a power-amplifier-output signal; said feedback signal is a first feedback signal derived from said power-amplifier-input signal; and said method additionally comprises, after down-converting said first feedback signal, down-converting a second feedback signal derived from said power-amplifier-output signal to generate said complex-return-data stream (see fig.2 and page 1 [0005-0006]).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 38- 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Sarca by U.S. Pub No 2005/0123066 A1.

As per claim 38, Sarca teaches a predistortion circuit for compensating linear distortion introduced by analog-transmitter components of a digital communications transmitter, said predistortion circuit comprising: a source of a complex-forward-data stream configured to digitally convey information (see figs.4-5 element 16); a quadrature-balance-adjustment section coupled to said complex-forward-data-stream source for providing a balanced- complex-forward-data stream to said analog-transmitter components (see figs. 4-5 element 20 and page 3, [0040-0041); a feedback section adapted to receive a feedback signal from said analog-transmitter components and to generate a complex-return-data stream (see figs.4-5 elements 22, 64 and 66 combined and page 4 [0060]); and a controller (see figs. 4-5 element 74) coupled to said feedback section and to said quadrature-balance-adjustment section and configured to implement one or more estimation-and-convergence algorithms (see page 4 [0051) in processing said complex-return-data stream to adjust said quadrature-balance-adjustment section to compensate for said linear distortion introduced by analog-transmitter components (see figs.4-5 element 7 and page 4 [0061] and page 5 [0069]).

As per claim 39, Sarca teaches wherein: said complex-forward-data stream exhibits a forward resolution (see figs 4-5 elements in path X); and said complex-return-

data stream exhibits a return resolution less than said forward resolution (see figs.4-5 elements in path y or feedback).

As per claim 40, Sarca inherently teaches wherein said feedback section generates said complex-return- data stream so that said return resolution is at most four bits less than said forward resolution (see page 4 [0051]).

As per claim 41, Sarca inherently teaches wherein: said quadrature-balance-adjustment section includes an adaptive equalizer (see pages 3-4, [0050-0051], [0059]); and said controller (see figs. 4-5 element 74)s configured to implement an estimation-and-convergence algorithm through said adaptive equalizer, wherein said estimation-and-convergence algorithm (see page 4 [0051)] of said adaptive equalizer converges upon filter coefficients (see page 5 [0063]) which cause said quadrature-balance-adjustment section to compensate for said linear distortion introduced by analog-transmitter components(see figs.4-5 element 72 and page 4 [0061] and page 5 [0069]).

As per claim 42, Sarca inherently teaches additionally comprising a programmable delay element (see page 3 [0047]) coupled between said complex-forward-data-stream source and said feedback section, said programmable delay element being configured to produce a delayed-complex-forward-data stream from said complex-forward-data stream, said delayed-complex- forward-data stream being temporally aligned with said complex- return-data stream (see page 5 [0067]).

As per claim 43, Sarca inherently teaches wherein: said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element(see page 3 [0047-0048]) and to said feedback section and having an output

coupled to said controller; and said controller implements an estimation-and-convergence algorithm through said correlator in order to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream (see page 5 [0067] and page 6 [0074-0075]).

As per claim 44, Sarca inherently teaches wherein: said one or more estimation-and-convergence algorithms are responsive to said complex-forward-data stream and to said complex-return-data stream(see figs. 4-5 element 74 and page 4 [0051)]; said complex-forward-data stream and said complex-return- data stream exhibit forward-error and return-error levels, respectively, with said return-error level being greater than said forward-error level (see page 3 [0046] and page 6 [0064]); and said one or more estimation-and-convergence algorithms are configured to transform increased algorithmic processing time into reduced effective-error level for said complex-return-data stream (see page 4 [0051, 0058] and page 5 [0062]) .

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-10, 17, 19, 21, 23, 25-28, 35, 47-49, 51-53, 55-56, 59-60 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rahman et al U.S. Pub No 2003/0174783 A1in view of Sarca U.S. Pub No 2005/0123066 A1.

7. As per claim 3, Rahman et al teaches all the features of the claimed invention except wherein said controller is configured to compensate for linear distortion in an RF-analog signal present at said input of said power amplifier, and then compensate for linear distortion in an amplified RF signal present at said output of said power amplifier.

8. Sarca teaches predistortion circuit controller configured to compensate for linear distortion in an RF-analog signal present at said input of said power amplifier, then compensate for linear distortion in an amplified RF signal present at said output of said power amplifier (see figs.4-5 element 7 and page 4 [0061] and page 5 [0069]).

9. It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Rahman as to provide a correction for linear distortions outside the up-conversion chain and determine adjustment needed in accordance with adaptation algorithm as taught by Sarca (see page 5 [0069]).

As per claims 4 and 47-48, Rahman et al teaches all the features of the claimed invention except wherein said equalizer section comprises: a non-adaptive equalizer configured to be programmed with filter coefficients; and an adaptation engine coupled to said non-adaptive equalizer and configured to implement an estimation-and-convergence algorithm which determines said filter coefficients.

Sarca teaches a non-adaptive equalizer configured to be programmed with filter coefficient (see fig.4 page 5 [0063]; and an adaptation engine (see fig.4 element 74 coupled to said non-adaptive equalizer and configured to implement an estimation-and-convergence algorithm which determines said filter coefficients (see page 4 [0051]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Rahman so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 5, Rahman and Sarca in combination would teach wherein said non-adaptive equalizer processes said complex-forward-data stream, and said adaptation engine is responsive to said complex-forward-data stream and said complex-return-data stream so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 6 and 25, Rahman and Sarca in combination would teach: said non-adaptive equalizer is a complex equalizer having an in-phase path, a quadrature path, an in-phase-to-quadrature path, and a quadrature-to-in-phase path; a first set of said filter coefficients is programmed in said in-phase and quadrature paths, and a second set of said filter coefficients is programmed in said in-phase-to- quadrature and quadrature-to-in-phase paths; and said adaptation engine accommodates a partial complex equalizer and has first and second paths, said first and second paths being configured in one mode to determine said filter coefficients for said in-phase and quadrature paths, and being configured in another mode to determine said filter coefficients for said in-phase-to-quadrature and quadrature-to- in-phase paths so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 7 and 55, Rahman and Sarca in combination would teach wherein said equalizer section implements an estimation-and-convergence algorithm to determine filter coefficients (see Sarca page 4 [0051] and page 5 [0063)) that compensate for said frequency dependent quadrature gain and phase imbalance so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 8, 10, 49 and 56, Rahman and Sarca in combination would teach: said estimation-and-convergence algorithm is responsive to said complex-forward-data stream and to said complex-return- data stream; said complex-forward-data stream and said complex-return- data stream exhibit forward-error and return-error levels, respectively, with said return-error level being greater than said forward-error level (see page 5 [0064]); and said estimation-and-convergence algorithm is configured to transform increased algorithmic processing time into reduced effective-error level for said complex-return-data stream so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 9, Rahman and Sarca in combination would teach wherein said estimation-and-convergence algorithm causes said equalizer section to converge at said filter coefficients after processing a multiplicity of samples from said complex-return- data stream so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 17 and 35 , Rahman et al teaches all the features of the claimed invention except: said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said feedback section and having an output coupled to said controller; and said controller and said correlator are configured to implement an estimation-and-convergence algorithm to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream.

Sarca teaches said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said feedback section and having an output coupled to said controller; and said controller and said correlator (see page 3 [0047-0048]) are configured to implement an estimation-and-convergence algorithm to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream (see page 5 [0067] and page 6 [0074-0075]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Rahman as to track the changes in the power amplifier characteristics and preserve the maximum achievable performance in time and with environment variations as taught by Sarca (see page 6 [0077]).

As per claims 19 and 23, Rahman and Sarca in combination would teach wherein: said equalizer section comprises an adaptive equalizer configured to determine filter coefficients (see Sarca page 5 [0063]) that compensate for said frequency dependent quadrature gain and phase imbalance; and said adaptive

equalizer increases correlation (see Sarca page 3 [0048]) between said delayed-complex-forward-data stream and said complex-return- data stream in determining said filter coefficients so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 21, Rahman and Sarca in combination would teach wherein said phase rotator (see Rahman page 5 [0042]) is configured to implement an estimation-and-convergence algorithm (see Sarca page 4 [0051] to determine an amount of phase rotation that compensates for said band-pass-filter delay so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 26, 27 and 51-52, Rahman et al teaches all the features of the claimed invention except wherein said controller is configured to cause said feedback section to monitor said first RF-analog signal while adjusting said first equalizer to compensate for linear distortion at said input of said power amplifier, then cause said feedback section to monitor said second RF-analog signal while further adjusting said first equalizer to compensate for linear distortion at said output of said power amplifier.

10. Sarca teaches wherein said controller is configured to cause said feedback section to monitor said first RF-analog signal while adjusting said first equalizer to compensate for linear distortion at said input of said power amplifier, then cause said feedback section to monitor said second RF-analog signal while further adjusting said first equalizer to compensate for linear distortion at said output of said power amplifier (see figs.4-5 element 7 and page 4 [0061] and page 5 [0069]).

11. It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Rahman as to provide a correction for linear distortions outside the up-conversion chain and determine adjustment needed in accordance with adaptation algorithm as taught by Sarca (see page 5 [0069]).

As per claims 28 and 53, Rahman and Sarca in combination would teach said first equalizer is adjusted to increase correlation between said second RF-analog signal and a first signal -84- responsive to said complex-forward-data stream and having a first bandwidth; and said second equalizer is adjusted to increase correlation between said second RF-analog signal and a second signal responsive to said complex-forward-data stream and having a second bandwidth wider than said first bandwidth as to provide a correction for linear distortions outside the up-conversion chain and determine adjustment needed in accordance with adaptation algorithm as taught by Sarca (see page 5 [0069]).

As per claims 59-60, Rahman and Sarca in combination would teach additionally comprising forming an error signal by combining said delayed- complex-forward-data stream and said complex-return-data stream so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 3 [0045-0048]).

As per claim 64, Rahman and Sarca in combination would teach: said quadrature-balancing activity is performed by an equalizer; said processing activity generates filter coefficients for said equalizer (see Sarca page 5 [0063]), said filter coefficients serving

as said quadrature balance parameters, and said filter coefficients causing said equalizer to compensate for linear distortion introduced by a portion of said analog-transmitter components upstream of a power amplifier; and said processing activity comprises revising said filter coefficients after compensating for said linear distortion introduced by said portion of said analog-transmitter components upstream of said power amplifier to additionally compensate for linear distortion introduced by said power amplifier as to provide a correction for linear distortions outside the up-conversion chain and determine adjustment needed in accordance with adaptation algorithm as taught by Sarca (see page 5 [0069]).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rahman et al U.S. Pub No 2003/0174783 A1in view of Rafie et al U.S. Pub no 20030058959.

As per claim 31, Rahman et al teaches a predistortion circuit additionally comprising: a local-oscillator-input port adapted to receive a local- oscillator signal from said analog-transmitter components, said local-oscillator signal exhibiting a local-oscillator frequency used by said analog-transmitter components for up-conversion (see fig.2 element 76).

However Rahman et al does not teach a synthesizer circuit for synthesizing a clock signal exhibiting a frequency equal to said local-oscillator frequency times 2N±I divided by four, where N is a positive integer selected to satisfy the Nyquist criteria for a bandwidth within which linear distortion is to be compensated; and -86- wherein said digital-subharmonic-sampling downconverter includes an analog-to-digital converter configured to sample said feedback signal at a rate determined by said clock signal.

Rafie et al teaches a PLL which well known in the art to be functionally equivalent to the claimed (synthesizer circuit) (see fig.11 element 1138) for synthesizing a clock signal (see fig.11 element clock) exhibiting a frequency equal to said local-oscillator frequency times 2N±I divided by four, where N is a positive integer selected to satisfy the Nyquist criteria for a bandwidth within which linear distortion is to be compensated; and wherein said digital-subharmonic-sampling downconverter includes an analog-to-digital converter (see fig.11 elements 1126 and 1128) configured to sample said feedback signal at a rate determined by said clock signal (see page 8 [0092]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Rafie into Rahman as to pre-compensate the linear amplitude and group delay distortion of the transmitter components as taught by Rafie (see page 8 [0096]).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Suzuki et al U.S. Patent No 7,170,342 B2 teaches linear power amplification.

15. Shirali U.S. Patent No 7,085,330 B1 teaches a method and apparatus for amplifier linearization.

16. Jeckeln et al U.S. Pub No 2002/0191710 A1 teaches an adaptive predistortion device.

17. McNichol U.S. Patent no 5,770,971 teaches distortion compensation.

18. Kim U.S. Pub No 2002/0181611 A1 teaches an analog quadrature modulator.

19. Ode et al U.S. Pub no 2005/0226346 teaches distortion compensation apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571 272 3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

1/30/2008

Emmanuel Bayard
Examiner
Art Unit 2611

EMMANUEL BAYARD
PRIMARY EXAMINER